IN THE SPECIFICATION

Please replace paragraph **[0028]** with the following amended paragraph:

[0028] FIG. 3 illustrates Peterson's algorithm for two threads (where n=2). This algorithm utilizes two conditions: a turn variable for ensuring that ~~that~~ a thread i, is placed in the processing queue, and a flag variable for indicating the status of another thread j. The status flag is a single-writer, as it may be written to by a single thread only (i.e., each thread may write to its own flag), while the turn variable is a multi-writer that may be written to by all threads. Both variables can be read by all threads.

Please replace paragraph **[0057]** with the following amended paragraph:

[0057] Similarly, it would be beneficial to use `prefetchnta` 624 instruction to bring the `flag[j]` 620 values into the closest cache level, Level 1 cache 612, of the CPU 606 [[600]]. In FIG. 6, the SSE `prefetchnta` 624 instruction is used to fetch the value of `flag[j]` 620, where j≠i, into the CPU's Level 1 cache 612. Note that the `prefetchnta` 624 bypasses the CPU's Level 2 cache 600. This helps to avoid polluting the Level 2 cache 600 with data that is going to be modified by another CPU/thread. A normal `movq` instruction 626 is used to read the `flag[j]` 620 value into a CPU register MM4 610 to perform the actual comparison operation as in the algorithm (see FIG. 3, line 6).

Please replace paragraph **[0058]** with the following paragraph:

[0058] Since `turn[k]` 616 [[614]] is a multi-writer variable, it does not benefit from the SSE instructions. It is read and written using the normal `movq` or `mov` instructions of the processor.